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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,638	03/30/2001	Ryou Nakagaki	16869P023300	6928

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EXAMINER	
SHAPIRO, JEFFERY A	

ART UNIT	PAPER NUMBER
3653	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,638	NAKAGAKI ET AL.	
	Examiner	Art Unit	
	Jeffrey A. Shapiro	3653	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6,9,11,28 and 30-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 6, 9, 11, 28 and 30-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 4, 6, 9, 11, 28 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stephan et al (US 6,338,001 B1). Stephan et al discloses the following.

As described in Claims 1, 6, 9, 11 and 30-32;

1. imaging an inspected object (204) (see col. 5, lines 10-16);
2. extracting an image of a defect candidate from an image obtained by said imaging step (see col. 5, lines 10-16);
3. classifying said extracted defect candidate image into a first category (at least one defect type) (see col. 5, lines 16-20, noting "defects are classed as to type and size");
4. classifying said extracted defect candidate into a second category (evaluation of defect criticality) (see col. 5, lines 20-27, noting that criticality is construed as a kill ratio);
5. displaying on a screen said extracted defect candidate image *together with first and second classification information, said first*

classification information relating to said first category, *said second classification information relating to* said second category;

(See figure 4, noting that it would have been obvious for the image data to be presented along with the defect data and kill ratio data, for example, which describes it, *as one ordinarily skilled in the art would recognize that* effective review and comparison of the chip defects with what an ideal example of such chip features should be (see col. 4, lines 65-67 and col. 5, lines 1-10) would require a visual representation of the particular defect so that appropriate changes can be made to the process or design of the chip);

6. *said step of classifying said extracted defect candidate image into said second category is performed by comparing a circuit pattern area and a defect area, said circuit pattern area being obtained from a reference image and said defect area being obtained from said imaging step*;

(Regarding using a comparison image, note that it would have been obvious to one of ordinarily skill in the art to use a comparison image from an ideal circuit pattern to compare to a defect area image. Otherwise, there is no way to determine the bounds of roundness, straightness, etc., of metal lines and structures created on the wafers, as described in Stephan et al at col. 1, lines 42-47. One of ordinary skilled in the art, in context to the teachings discussed in Stephan et al and cited above, would recognize that such comparison of an image of various chip defects

and an actual ideal chip feature would be required in order to determine whether or not the chip features which are defective are within acceptable tolerances. See also Chen et al (US 5,862,055), figure 3, step (304), incorporated by reference in Stephan et al at col. 2, lines 43-49. Note that each defect can be construed as a separate classification based on a classification code. See Chen at col. 1, lines 44-67, col. 2, lines 1-46, 63-67 and col. 3, lines 1-3. Also note as a further example, Gleason et al, at col. 2, lines 58-63 which describes use of a reference image (21) for comparison with defect image (22).

Further regarding Claim 32, note that evaluating overlap areas between the defect area and the reference circuit area are considered to be obvious, and that comparison of the two area images without overlay are considered to be functional equivalents.

As described in Claims 3, 4, 26 and 28;

7. said first category relates to defect criticality;

8. said second category relates to defect criticality;

9. said second category relates to defect type;

10. said first category relates to defect type;

(Note that regardless of whether or not the criticality or the defect type is determined first, the process result is substantially the same as Applicants' process. Note also that the location of a particular defect is captured by

the scanner, which one ordinarily skilled would find obvious to use for determining criticality, since criticality can be defined in terms of the location of the defect. See col. 1, lines 61-64.)

As described in Claim 9;

12. said second category relating to predicted yield from said inspected object (316);

3. Claims 2, 7, 10 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stephan et al (US 6,338,001 B1) in view of Gleason (US 6,456,899 B1). Stephan et al discloses the system described above. Stephan does not expressly disclose, but Gleason discloses the following;

As described in Claims 2, 7, 10 and 23-25;

6. said imaging of said inspected object is performed by illuminating and scanning an electron beam focused on said inspected object and detecting, in synchronization with said scanning, secondary electrons generated from said inspected object by said illumination (note that it is obvious to provide an electron beam for scanning, said electron beam necessarily producing secondary electrons from the surface it is directed at—see Gleason et al, for example, at col. 2, lines 58-63);

Both Stephan and Gleason are analogous art because they both concern automated semiconductor wafer inspection and defect classification systems.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have used an electron beam in the form of a scanning electron microscope (SEM) for inspecting the wafer.

The suggestion/motivation would have been to generate a reference image and a defect image. See col. 2, lines 58-63 of Gleason. Note also that Stephan discloses a semiconductor wafer inspection system, and that it would be obvious to one ordinarily skilled in the art to have used an SEM to obtain such images. See col. 2, lines 4-10 of Stephan.

Therefore, it would have been obvious to obtain the invention as described in Claims 2, 7, 10 and 23-25.

5. Claims 5, 8 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stephan et al (US 6,338,001 B1) in view of Nishimura et al (US 6,456,899 B1), further in view of Kumagai (US 5,394,481) and still further in view of Jarvis et al US 6,297,644 B1). Stephan et al discloses the system described above. Stephan does not expressly disclose, but Nishimura et al and Kumagai disclose the following;

As described in Claims 5 and 8;

> 11. said defect type includes one or more of the following: particle defects, flaw defects, circuit pattern short defects, circuit pattern open

defects and voltage contrast defects; (Note that an inspection system such as that of Steffan et al determines such defects, as one ordinarily skilled in the art would recognize them as well-known semiconductor circuit defects found in wafers during manufacturing. Note that these defects are considered to be functional equivalents of each other, at the very least. See also Nishimura et al, figure 3 and Kumagai et al, figure 9.)

Stephan does not expressly disclose, but Nishimura et al and Jarvis disclose the following;

As described in Claim 29;

13. calculating third information relating to voltage contrast of the defect candidate; (Note that this is considered to be a functional equivalent of other dimensional defects, and are related to shorts circuits or connection faults, as described in figure 3 of Nishimura et al. See also Jarvis et al (US 6,297,644), last four lines of abstract and figures 9a, 9b, 10a, 10b and 11, illustrating short circuit situations and col. 2, lines 66 and 67, col. 3, lines 1-9, and col. 7, lines 58-60, mentioning use of a scanning electron microscope (SEM) to perform such voltage contrast studies of defects. Note also that Stephan, at col. 2, lines 4-10, indicate that SEM is one of the pieces of equipment used for inspection of wafers.

Stephan, Nishimura, Kumagai and Jarvis are analogous art because they all concern automated semiconductor wafer inspection and defect classification systems.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have inspected a wafer for particle defects, flaw defects, circuit pattern short defects, circuit pattern open defects and voltage contrast defects.

The suggestion/motivation would have been to obtain "critical dimensions, that is, dimensions that can affect the performance of the semiconductor chip." See col. 1, lines 42-47 of Stephan. Note again, that figure 9 of Kumagai discloses various types of defects charted, such as holes, spots and breaks. Figure 3 of Nishimura discloses images of various connection faults and short circuits, said short circuits and connection faults construed as voltage contrast defects.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have calculated third information relating to voltage contrast of the defect candidate;.

The suggestion/motivation would have been to obtain "critical dimensions, that is, dimensions that can affect the performance of the semiconductor chip." See col. 1, lines 42-47 of Stephan. Note again, figure 3 of Nishimura discloses images of various connection faults and short circuits, said short circuits and connection faults construed as voltage contrast defects. Jarvis again discloses at col. 2, lines 50-67 and col. 3, lines 1-9, the use of "voltage contrast inspection" in order to identify catastrophic defects in semiconductor wafers.

Therefore, it would have been obvious to obtain the invention as described in Claims 5, 8 and 29.

Response to Arguments

6. Applicant's arguments filed 12/5/03 have been fully considered but they are not persuasive. Applicant asserts that the system of Stephan does not teach or suggest "displaying on a screen said extracted defect candidate image together with first and second classification information.." However, the prior art cited describes obtaining all of the information described in Applicant's claims. See above citations. Note in particular, col. 2, lines 6-10 of Stephan, which describes combining "linking data" with images of various defects. Note also Nishimura, figure 3, which shows images with their classification (kind of fault). As described above, there is ample motivation, suggestion and teaching in the prior art cited to, at the very least, allow one ordinarily skilled in the art to reasonably arrive at Applicant's claimed system.

With regards to the new limitations added to the independent claims, the above cited prior art again appear to meet them.

Therefore, Claims 1-11 and 23-32 are rejected.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey A. Shapiro whose telephone number is (703)308-3423. The examiner can normally be reached on Monday-Friday, 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald P. Walsh can be reached on (703)306-4173. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffrey A. Shapiro
Examiner
Art Unit 3653

September 27, 2004

DONALD P. WALSH
SUPERVISORY PATENT EXAMINER
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